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EXAMINER	
CHANG, EDITH M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/049,592	WURSTHORN, EDGAR	
	Examiner	Art Unit	
	Edith M. Chang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on January 12, 2006. These drawings are accepted.

Response to Arguments/Remarks

2. Applicant's arguments, see pages 10-12, filed January 12, 2006, with respect to the rejection(s) of claim(s) 1-5 and 9-10 under USC 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Williams.

Claim Objections

3. Claims 1-10 are objected to because of the following informalities:

Claim 1, line 3: "comprising a sampled and digitized data signal" should be "having a sampled and digitized data".

Since a phase detector as an apparatus comprises elements to construct the apparatus, not signal;

line 4: "having a delay stage" should be "comprising a delay stage".

Since the phase detector should comprise elements composed of;

line 8: "the phase error" should be "a phase error".

Since there is not antecedent basis for "the phase error";

lines 10-11: "one of the plurality of possible output values" should be " one of a plurality of possible output values";

line 13: "a plurality of possible output values" should be "the plurality of possible output values";

line 14: "the same output value" should be "a same output value".

Claims 5 & 6, line 3: "the data signal" should be "the sampled and digitized data signal".

Claim 6, line 2: "before rectification" should be (or is suggested to be changing to) "without rectification".

> Since in the Fig.5 discloses that the data signal is supplied parallel to a separating stage 55 and rectifier 51, not before rectification 51. The data signal is supplied to the separating stage 55 in which the data signal is separated into a positive and a negative path, and the rectifier 51 parallel.

Claim 9, line 3: "for a digital signal" should be "for the sampled and digitized data signal".

Claim 10, line 3: "the data clock signal in the data signal" should be "a data clock signal in the sampled and digitized data signal".

Claims 2-4 and 7-9 dependent on the objected claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 11: "the respective differential value" lacks antecedent basis. It is not clearly indicate whether it is the "a differential value" recited in line 6 of claim 1 or it is other?

line 13: "the said differential values" lacks antecedent basis, there is "a differential value" recited in line 6 of claim 1, but not "differential values".

Claim 2, line 5 (the last line): "the respective differential value" lacks antecedent basis.

Claim 8, line 5: "the complete data signal" lacks antecedent basis;

line 6: "the processing stages or comparison stages" does not clearly indicate which processing stages or comparison stages are; the positive path, the negative path, the further path or others?

Claims 3-7 and 9-10 dependent on the rejected claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 5,778,032) in view of Williams (US 5,592,125).

Regarding **claim 1**, in FIG. 12, Tanaka et al. discloses a phase detector (22-24 FIG.14) for a phase-locked loop (FIG.14, column 1, lines 35-45). Said phase detector comprises:

A delay stage (Delay Circuits 7 & 8) for delaying data signal (Sn) by one or more sampling clock periods;

A subtraction stage (subtracter 13, column 11, lines 14-16) producing a differential value of the undelayed (Sn) and the delayed (Sn-2) data signal;

A filter or control stage (Filter 15, VCO 6) receiving the differential value that a phase error can be tapped off.

However, Tanaka et al. does not explicitly specify a processing stage assigning the differential value to one of a plurality of possible output values.

Williams teaches the processing stage (Ternary Amplifier 123 FIG.1/606 FIG.6) located after the comparison stage (121 & 122 FIG.1) providing one of the plurality of possible output values to the differential value (column 6, line 52-59), wherein there are ternary values represented by (1,0), (0,1) and (0,0).

As Tanaka et al. having ternary values (FIG.5), at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have the processing stage (Ternary Amplifier 123 FIG.1/606 FIG.6 '125) taught by Williams located after the subtracter 13 (FIG.12 '032) in Tanaka et al.'s apparatus to detect the phase difference between the received data signal and the local clock (i.e., phase error) for the purpose of improving jitter performance (column 2, line 4-6 '125).

Regarding **claims 2** & **4**, the combined/modified apparatus discloses the subtraction stage is integrated in a comparison stage (FIG.6 '125) and deducts the delayed digital sample from the undelayed digital sample. .

Regarding **claim 3**, in FIG.12, Tanaka et al. discloses the phase error (output from Filter 15) with a differential value (from subtracter 13) and the multiplying with the previous values, feedback to VCO 6 to control the VCO such that the phase error is decreased (to lock), hence, Tanaka et al. disclosed the well-known PI (Proportional and Integral) control in the art to control the VCO.

Regarding **claims 9** & **10**, in FIG.12, Tanaka et al. discloses the phase detector integrated in a phase-locked loop circuit and the data signal delayed by one or more sampling clock periods corresponding to a data clock signal (FIG.3(c), column 7, lines 43-45 '032) in the data signal.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 5,778,032) in view of Williams (US 5,592,125) as applied to claim1 above, and further in view of Tanaka (US 5,452,326).

Regarding **claim 5**, though the combined/modified phase detector does not explicitly specify a rectifier for signal conditioning, however, in FIG.5, Tanaka teaches the rectifier (Absolute Value Detector 72) in a phase comparing unit 20 (FIG.2 '326). As Williams disclosing a positive input at 140 (FIG.2 A, column 7, lines 1-5 '125) and Tanaka et al. disclosing an absolute value in comparing undelayed and delayed samples (column 9, lines 20-29 & column 13, lines 26-30 '032) in the

combined/modified phase detector, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have the rectifier taught by Tanaka for signal conditioning in the combined/modified phase detector to represent sampling points to avoid error rate to be deteriorated (column 2, lines 34-44 '326) for the purpose of reproducing digital data (column 1, lines 5-10 '326).

Allowable Subject Matter

9. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcome the objection and the 112 rejection set fourth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least a phase detector for a phase-locked loop for digital input signals as a whole, the combination of elements and features, which includes the a separating stage in which a digital input signal is separated into a positive and a negative path as recited in the claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dawe (US 6,483,871 B1) describes a phase detector having a subtracter providing a differential value of a delayed signal (Phase Difference) and an undelayed signal (Reference) in Fig.3 & Fig.10.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed H. Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
March 23, 2006

KHAI TRAN
PRIMARY EXAMINER